A 0.5V Bulk-Input Operational Transconductance Amplifier with Improved Common-Mode Feedback

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Abstract—This paper presents the design of a two-stage pseudo-differential operational transconductance amplifier (OTA). The circuit was designed in a standard 0.18 μm, 0.5 V V_T digital CMOS process. An improved bulk-mode common-mode feedback (CMFB) circuit has been designed which does not load the OTA compared to previous design [2]. A self cascode load structure and partial positive feedback provide higher gain. The bulk terminals of all transistors have been biased to lower their V_T and maximize signal swing. The OTA operates at a supply voltage of 0.5 V and consumes only 28 μW of power. Rail-to-rail input is made possible by using the transistor’s bulk terminal as the input. For a load of 20 pF the OTA has a simulated DC gain of 65 dB, a gain-bandwidth product of 550 kHz, and a phase margin of 50°.

I. INTRODUCTION

As the feature size of CMOS technology continues to downscale, so too must the supply voltage [8]. The increase in demand for battery operated portable devices and implantable medical devices has put added pressure on lowering supply voltages. Devices such as hearing aids and remote sensors require very low power consumption, which is best achieved at supply voltages below 1V, with the transistors operating in the moderate inversion region [1][2]. A significant problem faced by analog designers is that as the technology size and supply voltage downscale, the transistor threshold voltage (V_T) remains fairly high [8]. Using standard analog design techniques, CMOS circuits will not operate correctly at supply voltages below 1V. Both the NMOS and PMOS require at least 2 V_T in order to be biased in moderate inversion. To meet this requirement a supply voltage of at least 2 V_T would be needed [8].

In order to circumvent the threshold voltage problem, a bulk-input technique is used, which allows for operation at supply voltages down to 0.5V. The MOSFET is a four-terminal device, but in normal circuit design the bulk terminal is always connected to the highest (or lowest) voltage in the circuit for a PMOS (or NMOS). This avoids forward biasing the bulk-source junction. At a supply voltage of 0.5V there is no longer a risk of forward biasing this junction, and the bulk terminal can be used without reservation [1][2]. The idea behind the bulk-input technique is that the gate of the input transistor can be biased in moderate inversion by applying the full supply voltage, and the bulk can be used as the input instead. This allows the input of the transistor to swing from rail-to-rail without decreasing the transistor inversion level.

The voltage applied to the bulk actually reduces the threshold voltage of the transistor, which increases the inversion level. One drawback of the bulk input technique is that the input transistor must sit in an n-well or p-well, so that its bulk is separate from the bulk of the rest of the transistors. This is not a problem in advanced technologies, which make use of triple-well structures. In triple-well processes both the NMOS and PMOS can have isolated bulk terminals.

This paper presents the design of a bulk-input pseudo-differential operational transconductance amplifier (OTA), which operates at a supply voltage of 0.5V. The circuit was designed using the IBM 0.18 μm 7RF technology, which has a threshold voltage of about 0.5V. This technology is a triple-well process, so the bulks of both the PMOS and NMOS transistors could be utilized.

A 0.5V OTA has been designed previously [2], but this design had a much lower gain due to the apparent loading of a resistive common-mode feedback (CMFB) circuit. This effect becomes more pronounced at lower bias currents. The bulk-mode CMFB circuit designed for our OTA overcomes this problem and allows for higher gain at even lower bias currents. The gain is further improved through a self-cascode structure and clever biasing of the bulk terminals of all transistors.

The following section describes the design of the circuit and is followed by an overview of the layout of the circuit and the simulated results. The paper concludes with a comparison to similar designs and a discussion of future work.

II. CIRCUIT DESIGN

A. Bulk-Input Pseudo-Differential Gain Stage

The design of the basic gain stage for the OTA is shown in Fig. 1. PMOS transistors M1A and M1B form a pseudo-differential pair with the positive and negative inputs applied to their bulks. The input transconductance of the stage is the bulk transconductance (g_mbs) of these transistors. The input common-mode voltage will decrease the V_T of the input transistors, which will increase their inversion level. The desired input common-mode voltage of 0.25V will lower the V_T of the transistors to about 380mV. This allows the gates of M1A and M1B to be biased at 100mV. The CMFB circuit described in the next section provides the gate bias for these transistors, based on the desired output common mode level.
The input pseudo-differential pair is loaded by NMOS transistor pairs M3 and M4. These transistors have their bulks biased at 0.25V, which lowers their threshold voltages. This makes it easier to keep the transistors in the moderate inversion region. Transistor M4 was added to increase the output impedance, which will increase the gain of the stage. Transistor pairs M3 and M4 could not be configured in a typical cascode configuration, as this would decrease the output swing, which is already limited by the low supply voltage. To increase the output resistance of the load without sacrificing output swing, transistor pairs M3 and M4 were designed in a self-cascode configuration. This configuration connects the gates of the two transistors together. M4 is operated in saturation and M3 is in non-saturation. As long as \((W/L)_4 >> (W/L)_3\), the circuit will behave like a single transistor M3 in saturation, with output resistance proportional to \((W/L)_4/(W/L)_3\). The \(V_{DS(sat)}\) of the two transistors remains about that of M3 [6]. By using a self-cascode load, the gain of the stage was increased by 6dB.

To further increase the gain of the stage, PMOS transistors M2A and M2B were added to form a cross coupled pair. These transistors have their gates biased at 100mV, which puts them in moderate inversion. Their bulks are used to form the cross coupled pair. This configuration adds a negative resistance to the output in the form of \(g_{mb2}^1\) [2]. By correctly sizing these transistors, the negative \(g_{mb2}\) term cancels out part of the denominator of the differential gain transfer function (1) and boosts the gain. The differential gain of the stage is:

\[
A_{diff} = \frac{g_{mb1}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{mb2}} \tag{1}
\]

Equation (1) shows how the bulk transconductance of transistors M2A and M2B can be used to boost the gain. The gain can be made very high by cancelling out most of the denominator, but the circuit will not be robust. Due to process and temperature variations, the transistor properties will change. Consequently, sufficient room for error must be maintained, so that \(g_{mb2}\) will never make the denominator negative. To ensure this, transistors M2A and M2B were sized so that their \(g_{mb}\) term canceled out only 50% of the denominator. This led to a gain boost of 6dB. The \(g_{ds3}'\) term in the gain equation is the \(g_{ds}\) of the self-cascode configuration of M3 and M4.

To form the two-stage OTA, two of the gain stages of Fig. 1 were cascaded to form the circuit in Fig. 2. Miller capacitor \(C_c\) was added in series with resistor \(R_e\) to increase the stability and move the right half plane zero to the left half plane. NMOS transistor M9 is used to set the biasing current in each of the stages. The second stage has a higher bias current than the first in order to increase the stability. Each stage required its own CMFB circuit, which is described next.

B. Bulk-Mode Common-Mode Feedback Circuit

A CMFB circuit is needed to prevent the output voltages from saturating to one of the power rails when the input common-mode voltage changes. The OTA from [2] had the previously discussed problem of its gain being decreased by the load that the CMFB circuit placed on the output. Fig. 3 diagrams the CMFB which was designed to overcome this problem.

The CMFB circuit in Fig. 3 is based on one discussed in [3]. The distinction is that the circuit in Fig. 3 uses the bulk terminals for the inputs of all the transistors. This allows the circuit to operate at a supply voltage of 0.5V. Transistors M11A and M11B sense the output common-mode voltage and turn it into current \(I_{cmfb}\). Transistors M12 and M13 form a bulk-input current mirror, which compares this current to \(I_{ref}\). The difference between \(I_{ref}\) and \(I_{cmfb}\) is fed back to the gate of the input transistors. This sets the output common-mode voltage to the reference voltage of 0.25V. Capacitor \(C_f\) in Fig. 1 is used to stabilize the CMFB circuit. The CMFB circuit does not require the use of a resistor and does not load the output.

![Figure 1. Bulk-Input Pseudo-Differential Gain Stage](image1)

![Figure 2. Two-Stage Bulk-Input Pseudo-Differential OTA](image2)
III. PHYSICAL LAYOUT

The physical layout of a circuit can influence the final performance of the chip. One major concern in low power circuits is that the leakage currents have a greater effect on circuit performance, due to the low biasing currents. This effect is further increased when the bulk terminal is used to carry the signal. The bulk terminals of the PMOS transistors used for the circuit sit in the substrate. Any leakage current in the substrate could influence the signal at the bulk terminal. To shield the bulk terminals from leakage currents, n-well guard rings were placed around each PMOS transistor. The NMOS transistors did not need guard rings because they were already guarded by the triple-well.

Other standard analog layout techniques, such as common centroid and unit-size transistors, were also used to increase the circuit performance. For clarity, the layout of the OTA is shown in Fig. 4 without interconnections to pads. The first and second stages of the OTA can be seen, with the second stage being larger than the first due to its higher bias current. The six capacitors can be seen on the right side and top left corner of the layout.

IV. SIMULATION RESULTS

The circuit was designed in IBM 0.18µm CMOS technology using the Cadence design environment. Final chip layout has been completed with all the pad connections. The layout was extracted to include both resistive and capacitive parasitics. The following simulation results were obtained using the Spectre simulator on the extracted layout, with pad connections and wire bond parasitics included.

Referring to Fig. 2, a biasing current of 10µA was input through M9 and mirrored to the NMOS loads of each stage. This current was also mirrored to the NMOS transistors of the CMFB circuit. The NMOS transistors had different sizes, which made their bias currents different. The bias currents of the first and second stages were 5µA and 20µA, respectively. The bias currents of the CMFB circuits of the first and second stages were 1µA and 4µA, respectively. These bias currents made the power consumption of the OTA 28µW.

The open-loop AC response of the OTA is shown in Fig. 5. The DC gain of the circuit is 65dB. With a 10pF load on each output (20pF total), the gain-bandwidth product is 550kHz and the phase margin is 50°. Compared to the OTA designed in [2], the DC gain was increased by 13dB while obtaining a four times reduction in power consumption.

The OTA was simulated in closed-loop unity-gain configuration. The AC response of this configuration is shown in Fig. 6. The gain-bandwidth product is 475KHz. The response of the unity-gain closed-loop configuration to a square wave input is shown in Fig. 7. The output signal displays good phase margin with no ringing.

Other important parameters include: 1) the rising and falling slew rates, which were 0.49V/µs and 0.30V/µs, respectively, 2) the CMRR and PSRR at 5kHz, which were 86db and 67dB, respectively, 3) the input referred noise, which was \( \frac{675}{\sqrt{10}} \) Hz at 10kHz, and \( \frac{160}{\sqrt{10}} \) Hz at 550kHz, 4) the input current at 27°C, which was 1.2nA, 5) the output clipping level, which was 395mV peak-to-peak, and 6) the output amplitude for 1% third-order harmonic distortion, which was 375mV peak-to-peak.

A summary of the simulated results is shown in Table I.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>0.5V</td>
</tr>
<tr>
<td>Open-Loop DC Gain</td>
<td>65 dB</td>
</tr>
<tr>
<td>Open-Loop GBW</td>
<td>550 kHz</td>
</tr>
<tr>
<td>Open-Loop Phase Margin</td>
<td>50°</td>
</tr>
<tr>
<td>Closed-Loop GBW</td>
<td>475 kHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>28 µW</td>
</tr>
<tr>
<td>CMRR @ 5 kHz</td>
<td>86 dB</td>
</tr>
<tr>
<td>PSRR @ 5 kHz</td>
<td>67 dB</td>
</tr>
<tr>
<td>Slew Rate ( \uparrow )</td>
<td>0.49 V/µs</td>
</tr>
<tr>
<td>Slew Rate ( \downarrow )</td>
<td>0.30 V/µs</td>
</tr>
<tr>
<td>Input Ref. Noise @ 10 kHz</td>
<td>( \frac{675}{\sqrt{10}} ) Hz</td>
</tr>
<tr>
<td>Input Ref. Noise @ GBW</td>
<td>( \frac{160}{\sqrt{10}} ) Hz</td>
</tr>
<tr>
<td>Load Capacitor</td>
<td>20 pF</td>
</tr>
<tr>
<td>Input Current @ 27°C</td>
<td>1.2 nA</td>
</tr>
<tr>
<td>Output Amp. For 1% HD3</td>
<td>375 mV p-p</td>
</tr>
<tr>
<td>Output Clipping Level</td>
<td>395 mV p-p</td>
</tr>
<tr>
<td>Layout Area</td>
<td>0.052 mm²</td>
</tr>
</tbody>
</table>
Future work will entail using the OTA to build higher level circuits for use in low power sensors.

**REFERENCES**


**V. CONCLUSION**

This paper has presented the design of a bulk-input OTA, which operates at a supply voltage of 0.5V. The design incorporates a new bulk-mode CMFB, which no longer loads the OTA as in [2]. This new CMFB scheme, along with the use of a self cascode load, greatly improves the gain of the circuit. Clever biasing of the bulk terminals of all transistors has lowered their $V_t$ and maximized signal swing. Final layout of the OTA on chip has been completed and been verified in the Cadence design environment. The chip has been submitted to MOSIS for fabrication and will be tested on a PCB to confirm the simulation results.