DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

PH.D. QUALIFYING EXAM

JANUARY 2020
EE-18 - Electromagnetic Fields and Waves

Note: if you do not have an equation, make an attempt to derive it. Otherwise, indicate how you would solve the problem if you had the information you are missing and describe as best you can what the answer should be, and check that your units are correct.

Part 1 (70 pts)
There is a form of transmission line known as a “Goubau Line.” This transmission line can be considered a simple copper wire of radius \( R \) surrounded by air. Find the Electric field, \( \mathbf{E} \)-field, (using Gauss’s Law), and magnetic field, \( \mathbf{B} \)-field, (using Ampere’s Law) inside of the air. Then find the Electric Potential (V) outside the conductor. Note, when using these laws in matter, you first need to find the \( \mathbf{H} \)-Field and \( \mathbf{D} \)-field. For now let’s assume there is a charge-per-unit-length of \( +\lambda \) on the line with this charge flowing with a constant velocity to form a current of \( +I_0 \). This part should be done purely symbolically, show all work.

Part 2 (30 points)
Using the facts that the relative permittivity of Air is approximately 1 (Note: \( \varepsilon_0 = 8.854 \times 10^{-12} \, F/m \) and \( \mu_0 = 4\pi \times 10^{-7} \, H/m \)). What are the loss-less lumped element circuit model components (L and C) for a unit length of the Goubau line? What is the characteristic Impedance of this transmission line, and what does it mean? Hint: you will need to find the energy stored in the magnetic field to find \( L/\ell \). This part should also be done symbolically, if you cannot get a part, do your best to explain your process. Simplify, your expressions down to the base variables if possible. Your solutions should be in terms of: \( a, b, \mu_0, \mu_r, \) and \( 2\pi \).
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Solution:

\[ Q_{\text{free}} = \lambda l = \int D \cdot da \]

\[ \lambda l = \int_0^l \int_0^{2\pi} D r d\theta dz = 2\pi D r l \]

\[ D = \frac{\lambda}{2\pi r} \hat{r} \text{ so } E = \frac{D}{\varepsilon_0 \varepsilon_r} = \frac{\lambda}{2\pi \varepsilon_0 \varepsilon_r r} \hat{r} \]

\[ V = -\int E \cdot dl = -\int_a^r \frac{\lambda}{2\pi \varepsilon_0 \varepsilon_r r} dr = \frac{\lambda}{2\pi \varepsilon_0 \varepsilon_r} \ln \frac{r}{a} \]

\[ I_{\text{encl}} = I_0 = \oint H \cdot dl \]

\[ \oint H \cdot dl = \int_0^{2\pi} H r d\theta = 2\pi r H \text{ so } H = \frac{I_0}{2\pi r} \hat{\theta} \]

\[ B = \mu H \text{ so } B = \frac{\mu_0 \mu_r I_0}{2\pi r} \hat{\theta} \]

Part 2:

\[ C = \frac{Q_{\text{free}}}{V} = \frac{\lambda l}{2\pi \varepsilon_0 \varepsilon_r \ln \frac{r}{a}} \text{ so } C \frac{l}{\lambda} = \frac{2\pi \varepsilon_0 \varepsilon_r}{\ln \frac{r}{a}} \text{ as } a \to \infty \frac{C}{l} \to 0 \]

\[ W_2 = \frac{1}{2} \int \mu |H_2|^2 d\tau = \frac{\mu I_0^2}{8 \pi^2} \int_0^l \int_0^{2\pi} \int_a^r r dr d\theta dz = \frac{\mu_0 \mu_r I_0^2 l}{4 \pi} \ln \frac{r}{a} \]

\[ L = \frac{2W_m}{I_0^2} = \frac{\mu l}{2\pi} \left[ \ln \left( \frac{r}{a} \right) \right] \text{ so } \frac{L}{\mu_0 \mu_r I_0^2} = \frac{2\pi}{2\pi} \left[ \ln \left( \frac{r}{a} \right) \right] \]

\[ Z_0 = \sqrt{\frac{L}{C/l}} = \sqrt{\frac{\mu_0 \mu_r}{2\pi} \ln \left( \frac{b}{a} \right) \left( \frac{\ln \frac{r}{a}}{2\pi \varepsilon_0 \varepsilon_r} \right)} = 2\pi \ln \frac{r}{a} \sqrt{\frac{\mu_0 \mu_r}{\varepsilon_0 \varepsilon_r}} \]

as \( a \to \infty \) \( Z_0 \to 0 \) so for a Goubau line to make sense, you can’t use a low loss approx!
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Grading Rubric (Total: Part 1) 70, Part 2) 30

\[ Q_{\text{free}} = \lambda l \] (10 points)

\[ D = \frac{\lambda}{2\pi r} \hat{r} \] (10 points)

\[ E = \frac{D}{\varepsilon_0 \varepsilon_r} \hat{r} \] (10 points)

\[ V = \frac{\lambda}{2\pi \varepsilon_0 \varepsilon_r} \ln \frac{r}{a} \] (10 points)

\[ I_{f\text{enc}} = I_0 \] (10 points)

\[ H = \frac{I_0}{2\pi r} \hat{\theta} \] (10 points)

\[ B = \frac{\mu_0 \mu_r I_0}{2\pi r} \hat{\theta} \] (10 points)

In all cases the correct method (initial equation will be worth ½ the points and the solution ½ the points. Partial credit maybe awarded depending on the severity of any math error.

If the solution is correct for the equation used full points can be given as long as dimensional analysis gives the correct units. If a "random" formula is chosen with no equations, no points will be awarded. However, this formula can be used for other parts as long as the units stated are correct. **If a correct answer is given with vector direction, 3/4 points will be awarded.**

**Note:** As per directions, a correct explanation to “describe best you can what the answer should be, and check that your units are correct.” Will net **1 pt out of 2 pts** for the equation portion of the rubric.

Total Part 70 pts

\[ C = \frac{2\pi \varepsilon_0 \varepsilon_r}{\ln \frac{r}{a}} \] (10 points)

\[ L = \frac{\mu_0 \mu_r}{2\pi} \left[ \ln \left( \frac{r}{a} \right) \right] \] (10 points)

\[ Z_0 = 2\pi \ln \frac{b}{a} \sqrt{\frac{\mu_0 \mu_r}{\varepsilon_0 \varepsilon_r}} \] (5 points)

Must contain loss to make sense (5 points)

In all cases the correct method (initial equation will be worth ½ the points and the solution ½ the points. Partial credit maybe awarded depending on the severity of any math error.
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If the solution is correct for the equation used full points can be given as long as dimensional analysis gives the correct units. If a "random" formula is chosen with no equations, no points will be awarded. However, this formula can be used for other parts as long as the units stated are correct. **If a correct answer is given with vector direction, 3/4 points will be awarded.**

**Note:** As per directions, a correct explanation to "describe best you can what the answer should be, and check that your units are correct." Will net **1 pt out of 2 pts** for the equation portion of the rubric.  
**Total Part 30 pts**
EE-113/EE-114 - Semiconductors

Note: if you do not have an equation make an attempt to derive it. Otherwise, indicate how you would solve the problem if you had the information you are missing and describe best you can what the answer should be, form and function.

1) For a standard high-electron-mobility transistor (HEMT) answer the following questions:
   a. Draw a cross-section of a HEMT indicating all of the layers, approximate doping levels, and their purpose.
   b. Draw the band diagram for the diode. For simplicity, consider using the GaAs/AlGaAs heterojunction-based HEMT for your material system, but you may use any material set of your choice as long as you clearly indicate it. On the drawing, label the P, N, depletion, and any other special regions; as well as, the directions of carrier flows and the barriers to this flow.
   c. As a function of gate voltage show how the band diagram changes including the direction of carrier flows.

2) A photovoltaic cell is a standard PN or PIN photodiode. For the purposes of this question assume the structure is a GaAs homojunction PV cell consisting of five layers with dopant concentrations of n++/n/I/p/p++, with n++ being the top layer. Below is a circuit equivalent model for a photovoltaic cell.
   a. Draw the approximate Dark and Light JV curves for the PV cell. Label the points on the curve where the load is shorted versus an open circuit. Also, note the point on the curve that represents the optimal load.
   b. What is the purpose of the n++ and p++ layers?
   c. As you increase the following parameters what beneficial and detrimental effect does it have? If relevant, show how it affects the JV curve.
      i. Thickness of the intrinsic region
      ii. Thickness of the emitter (n) region
      iii. Doping of the emitter (n) region
      iv. Thickness of the absorber (p) region
      v. Doping of the absorber (p) region
      vi. Bandgap
      vii. Spacing between front-side contact grid
   d. Light is an electromagnetic wave, an AC signal, so why does the PV cell give a DC signal?
Finish the connections of the device (the 4 unspecified inputs, they could be external or intermediate inputs) and the characteristic table below to make it a rising-edge-triggered D-FF with Preset (S) and Reset (R).

(a) What are the hold time and setup time of the flip-flop? Assume each gate has a propagation delay of 10 ns.

(b) Let’s define the propagation delay of the FF as the period of time from the rising edge of the clock to the new state becomes stable. What is the propagation delay of this FF?

(c) How long does it take to reset the flip-flop using R?

(d) List three methods to reduce a sequential machine.
EE-128 - Operating Systems

Deadlock prevention is an important issue in Multiprocessing Operating System. Prove that the following deadlock prevention strategy works for any number of processes:

a. Define a linear ordering of resources. If a process has been allocated resource $i$ then it may subsequently request only those resources following $i$ in the ordering.
ES-3/EE-21 - Circuit Theory

a) Treat the operational amplifier in the circuit below as *ideal* and solve for \( V_o \).

b) Treat the op amp as a *non-ideal* device that is powered by \( V_{CC} \) and \( V_{EE} \); describe several ways in which your answer in part a) will change.

\[ V_i = 2\cos(2\pi \times 10^6 t) \text{ volts} \]

\( R_L = R_1 = 0.5R_2 = 1 \ \Omega \)

\( C_1 = 9\mu F; \ C_2 = 11\mu F; \ \text{Q}=CV \)

\( V_{CC} = -V_{EE} = 5 \text{ volts} \)
Below is an RLC circuit with an input voltage \( u(t) \) and output voltage \( y(t) \).

1. Write a state-space model for this system.
2. Is this system BIBO-stable? Demonstrate why or why not. If it is only BIBO-stable for some values of \( r/l/c \), find the range of those values.
3. Write a transfer function corresponding to this system.
4. Suppose we wanted to use this circuit with feedback control to build an oscillator. Design a feedback controller using the output \( y(t) \) such that the closed-loop system oscillates at 1kHz (i.e., the poles of the system are at \( \pm 1000 \)).
   It is sufficient to draw a block diagram and calculate the gain(s) or transfer function for the controller.
   You don’t need to implement the controller with circuit components.
Problem 1 - Basic Caches (7 pts)
A memory hierarchy with a direct mapped L1 cache (with no other caches in the system) uses 4-byte words and 8-bit physical addresses. The system is running a test application accesses the following memory addresses (8-bit addresses), shown in hex: 0x04, 0x10, 0x1C, 0x0C, 0x14, 0x08, 0x00. The clock rate is 2GHz; access time for L1 hits is 4 cycles, and for L1 misses is 20 cycles.
The L1 cache has the following parameters:

- Word size 4 bytes
- Block size 8 bytes
- Cache capacity: 32 bytes
- Associativity: direct mapped
- Physical address size: 8-bits

Please provide the following:

a. Tag, index, and offset bits for each address
b. Record if each access was a hit or miss and the final contents of the cache
c. Average memory access time (AMAT)

Problem 2 - Advanced Caches (6pts)
Time to design a better memory hierarchy. Given that we must keep the total amount of cache at 32B, which of these two options do you think would most improve the performance of the cache above specifically for the address sequence just given:

a. Doubling the block size to 4 words rather than 2 (while keeping the cache direct mapped)
b. Making the cache 2-way set-associative and reducing the block size to 1 word.

You should justify your choice with intuitive reasons – not just with “because it comes up with fewer misses.”

Next, for whichever cache choice you did not pick, design an address sequence that would make that cache more attractive.
Problem 3 - Virtual Memory (6 pts)

A processor has:
- a 40-bit virtual-address space with 4KB pages
- 1 GB of physical memory
- a 1KB two-way set-associative cache with one-word blocks.

For this processor, **fill in the block diagram below.** Connect up the wires as needed, and label each wire to show which bits of the address go where (**be sure to label which bits are in each wire**). We’ve shown two separate muxes for the read datapath – the top one picks which of the two ways to read (and is one-hot), and the bottom one picks which byte of the word to use. Neither the cache’s valid bits nor its store datapath are shown; you can ignore them both.

Next, answer this question: is this cache virtually indexed and physically tagged? Why or why not?
EE-126 - Computer Engineering

Problem 4 - Pipelines (6 points)
The following code segment will execute on a 32-bit MIPS processor with the following features:

- We have a six-stage pipeline: instruction fetch (IF), instruction decode (ID), two execute stages (E1 and E2), memory access (M), and write back (WB). I.e., the ALU takes two cycles to perform arithmetic operations rather than just one – but hopefully runs at a correspondingly higher clock frequency.
- The processor has forwarding and bypassing logic. It can forward data from the E2/M and M/WB pipeline registers directly to the E1 ALU inputs. It does not forward from the E1/E2 register to anywhere, since there is no useful data to forward from there. It can also forward from the M/WB pipeline register directly to the M-stage store data if needed.
- The processor supports simple static branch prediction by always predicting taken.
- Branches are resolved in the E2 stage. I.e., the CPU makes a final determination on whether or not the branch should be taken in the branch’s E2 stage, and then acts on it (e.g., fetching a new instruction, squashing other instructions, etc.) in the following cycle. You can squash any instructions that you need; not just ones going from IF to ID.

Show how the following code segment is executed on the processor with a pipeline table like the one below. Assume that the branch winds up being taken. Note that because of the branch, not all of the instructions listed in the table may actually be executed or even fetched.

```
LW   $t1, 0($t0)
BEQ  $t1, $t2, LABEL1
ADDI $t1, $t1, $t5
SUB  $t2, $t2, $t5
LABEL1: ADD $t2, $t2, $t5
LW   $t3, 4($t2)
SW   $t3, 8($t0)
```

| Cycle -> | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|----------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|
| LW $t1, 0($t0) | IF | ID | E1 | E2 | M | WB |
| BEQ $t1, $t2 |    |    |    |    |    |    |
| ADDI $t1, $t1, $t5 |    |    |    |    |    |    |
| SUB $t2, $t2, $t5 |    |    |    |    |    |    |
| ADD $t2, $t2, $t5 |    |    |    |    |    |    |
| LW $t3, 4($t2) |    |    |    |    |    |    |
| SW $t3, 8($t0) |    |    |    |    |    |    |
Part 1
Assume all the transistors are in saturation and have identical $g_m$ and $r_o$. What is the expression of the low frequency gain and the output impedance for the following circuit?

Part 2
Plot the frequency response, both magnitude and phase, for the voltage gain of following amplifier. Assume transistor is in saturation and DC biasing is implicit.
$k_n = u_n C_{ox}(W/L)= 1\text{mA/V}^2$, channel length modulation $= 0.01 \text{ V}^{-1}$, $C_{gs} = 1\text{pF}$ (where $\text{pico}= 10^{-12}$).

Ignore $C_{gd}$ and $C_{db}$.
EE-107 - Communications Systems

Question 1
A message signal \( m(t) = \text{sinc}(t/T) \) with \( T = 0.5 \) ms is used as the input to a conventional amplitude modulator with a carrier frequency \( f_c = 100 \) kHz and carrier amplitude of 2V. The transmitted signal is \( x(t) = 2[1+m(t)] \cos[2\pi f_c t] \).

The function \( \text{sinc}(x) \) is defined as \( \frac{\sin(x)}{x} \) and has a minimum value of -0.22.

a) What is the value of the modulation index, defined such that a modulation index of 1 is the threshold over which there is overmodulation?

b) Write an expression for the Fourier transform of the modulated signal.

c) Sketch a plot of this spectrum (amplitude only), labelling both amplitude and frequency axis and also indicating the area of any impulse functions.

d) This signal is now multiplied by a unit amplitude replica of the carrier. Sketch the spectrum of the resulting signal.

e) The resulting signal from part d is now passed through an ideal lowpass filter with a bandwidth of 100 Hz. Write an expression for the filter output signal (in the time domain), and sketch a plot of it, labelling significant points on the time and amplitude axes.

Question 2
An orthogonal binary modulation system transmits sinusoidally modulated rectangular pulses. The received pulses are:

\[ s_1(t) = 0.001 \cos[2 \times 10^6 \pi t \left( \frac{t}{10\mu s} \right)] \left\{ \begin{array}{ll} 1 & \text{for a "1" (volts into a 1Ω resistor)} \\ 0 & \text{for a "0" (volts into a 1Ω resistor)} \end{array} \right. \]

\[ s_0(t) = 0.001 \sin[2 \times 10^6 \pi t \left( \frac{t}{10\mu s} \right)] \left\{ \begin{array}{ll} 1 & \text{for a "1" (volts into a 1Ω resistor)} \\ 0 & \text{for a "0" (volts into a 1Ω resistor)} \end{array} \right. \]

a) Draw a block diagram of an optimal correlator-based receiver

b) The receiver also gets additive white Gaussian noise with a power spectral density of \( N_0/2 \). (The spectrum includes both positive and negative frequencies.) If \( N_0 = 10^{-12} \) W/Hz, what is the bit error probability for this receiver?

c) Now suppose the carrier frequency of the pulse is increased from 106 to 107 Hz. What is the new bit error probability?
Below is a table of the Q function, which you can use for bit error probability calculations. When using the table, you can just pick the nearest entry.

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<th>$x$</th>
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EE-23 - Linear Systems Theory

Let $x[n]$ be a discrete time signal obtained from a real valued, continuous time signal $x(t)$ via

$$x[n] = \int_{(n-1/2)T}^{(n+1/2)T} x(t) dt$$  \hfill (1)

where $T$ is a real-valued, non-negative number.

1. It is claimed that we can equivalently write (1) as

$$x[n] = \int_{-\infty}^{\infty} x(nT - \tau) s(\tau) d\tau.$$  

Identify the signal $s(t)$ for which this equality holds.

2. For the $s(t)$ determined above, prove that $\int_{-\infty}^{\infty} x(nT - \tau) s(\tau) d\tau = \int_{-\infty}^{\infty} s(\tau - nT) x(\tau) d\tau$. Does this equality hold for any $s(t)$? If yes explain, if not, for what class of $s(t)$ will it hold?

3. Show that the sampling theorem does not hold for this approach to discretization by providing a bandlimited signal which cannot be recovered from its samples and proving this to be the case.

4. What is the maximum bandwidth of $x(t)$ which will allow for the perfect recovery of the continuous signal from $x[n]$? For signals satisfying this requirement, provide a detailed description of the system which you would use for recovering $x(t)$. The result of your analysis should be an interpolation formula like the one associated with the Shannon sampling theorem; i.e.

$$x(t) = \sum_n x[n] g_n(t)$$

Your $g_n(t)$ should be written in terms of the inverse Fourier transform of some filter.

5. With $T = \frac{\pi}{32}$ and $x(t) = x_b(t) \cos(72t)$, determine the largest bandwidth of $x_b(t)$ such that $x(t)$ could be recovered from its samples and discuss the system you would use for accomplishing this task.
EE-104 - Probability and Statistics

In this problem consider a stick of unit length that is broken once, with the uniform probability distribution for the location of the break. Let the length of the shorter piece be $X$.

a) Find the expectation $E[X]$

b) Find the expectation for the product of $X$ and the longer piece.

c) Extra credit (do this time permitting) – find the expectation of the ratio of $X$ and the longer piece.

d) Consider now a rectangle whose sides are the two pieces of the (broken) stick. What is the probability that its area is larger than 1/8.

e) Consider now a sequence of independent, identically distributed (iid) samples $X_i$ for $i = 1, 2, ...$ At each $i$, we make a random, equally likely choice between the shorter and the longer piece and call that random variable $Z_i$. Let

$$S_n = \sum_{i=1}^{n} Z_i$$

Find the expectation and variance of $S_n$

f) Consider now

$$B_n = \frac{\sum_{i=1}^{n} X_i}{n}$$

1. What is a good approximation for $B_{1000}$?

2. Assuming a normal (Gaussian) approximation is used, what is $n$ such that the probability $P(B_n < 0) < 10^{-6}$
COMP-11/COMP-15 - Programming

Suppose we have the following (partial) class definition for a binary search tree:

```cpp
template <typename T>
class BTree
{
    public:
        // Return the number of leaf nodes in the tree
        int countLeafNodes() const;

        // Destructor, which cleans up all memory
        ~BTree();

        // Other methods...

        // Assignment operator, which makes a deep copy of the tree
        const BTree<T>& operator=(const BTree<T>& rhs);

    private:
        Node* mRoot = nullptr;
};
```

1. Write an implementation for the function `countLeafNodes()`, which returns the total number of leaf nodes in the tree.

2. Write the destructor for the `BTree` class, which cleans up all of the memory from dynamically-allocated Nodes. You’re welcome to write one or more helper functions if it makes your code simpler.

3. Write the assignment operator for the `BTree` class, which makes a deep copy of the tree. Again, you’re welcome to use helper functions (including any you wrote above) if it makes things easier. *Hint: Don’t get so caught up in the binary search tree details that you forget to do the assignment operator details correctly.*

4. A hash table is $O(1)$ for both insertion and lookup/retrieval, while a binary tree is $O(\log(N))$. Given this, why would you ever use a binary tree instead of a hash table?
EE-103 - VLSI

Topic 13:
Use the following 180nm CMOS device parameters from the VK Technologies foundry for the problems below, unless otherwise specified.

1. VDD = 1.8V
2. Nominal Threshold Voltages: \( V_{Tn} = 0.4 \text{ V}, V_{Tp} = -0.4 \text{ V} \)
3. Gate Oxide \( T_{OX} = 50\text{Å} \)
4. Carrier Mobilities: \( \mu_n = 700\text{cm}^2/\text{Vs}, \mu_p = 350\text{cm}^2/\text{Vs} \)
5. Diffusion Capacitances:
   a. \( C_{\text{bottom}} \): Capacitance of the junction between the body and the bottom of the source/drain with units of capacitance per unit area. \( C_{\text{bottom}} = 1\text{fF}/\text{um}^2 \)
   b. \( C_{\text{bsw}} \): Capacitance of the junction between the body and the sidewalls of the source/drain with units of capacitance per unit length. \( C_{\text{bsw}} = 0.5\text{fF}/\text{um} \)
6. Substrate doping concentration: \( N_A = 2 \times 10^{17}/\text{cm}^3 \)
7. Channel length modulation parameter \( \lambda = 0 \)
8. Minimum Source/Drain diffusion lengths \( L_{\text{diff}} = 0.5\text{um} \) for all NMOS and PMOS transistors

<table>
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<tr>
<th>Gate type</th>
<th>Number of inputs</th>
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<td>Inverter</td>
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<tr>
<td>NAND</td>
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<tr>
<td>XOR, XNOR</td>
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<table>
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<th>Gate type</th>
<th>Number of inputs</th>
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</thead>
<tbody>
<tr>
<td>Inverter</td>
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<tr>
<td>NAND</td>
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<tr>
<td>XOR, XNOR</td>
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Logical effort          Parasitic delay

**Problem 1** - Consider a 2-input NOR gate with gate length \( L = 180\text{nm} \) and gate width \( W = 500\text{nm} \) for all NMOS and PMOS transistors:

a. Sketch the transistor level circuit diagram and label the input and output signals.
b. Sketch the physical layout. In addition to the input and output signals, label the polysilicon, diffusion, contact, and metal layers. (Note: You do not have to draw to scale.)
c. Write an expression for \( C_{\text{out}} \), the total capacitance at the output node for the NOR gate. Your expression should be in terms of \( C_{\text{bottom}}, C_{\text{bsw}}, L_{\text{diff}}, L, \) and \( W \). (Note: You do not have to include the metal interconnect capacitance at the output node.)
d. Use the linear delay model to compute the normalized delay of the NOR gate driving 4 copies of itself.
Problem 2 - Consider the following circuit with 2 NOR gates and a delay element consisting of a CMOS transmission gate and capacitor C. Assume the delay element introduces a delay of 10ns and the delay through the NOR gates is negligible. The input signal \( b \) is a square pulse with period of 100ns and 50% duty cycle as shown below.

Sketch the output waveform from 0 to 200ns for the following cases:

Case 1: Input \( a = 0, s = 0 \)
Case 2: Input \( a = 1, s = 0 \)
Case 3: Input \( a = 0, s = 1 \)
Case 4: Input \( a = 1, s = 1 \)
Problem 3 - The parameters are given for the circuit components in the figure below. The clock frequency is 10MHz. Assume there is zero clock skew and no time borrowing takes place.

<table>
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<th>Setup Time</th>
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<td>35ns</td>
<td>30ns</td>
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</table>

NAND gate delay: 20ns
NOR gate delay: 25ns
Inverter delay: 10ns

a. Will this circuit work correctly? Explain, and find the magnitude of the violation, if any.
b. What is the maximum clock frequency at which the circuit will operate correctly?